REMARKS/ARGUMENTS

In the Office action, claims 7, 26, and 32 were objected to because of the recitation "vice versa" at the last line of each claim. In response to the examiner's suggestion, the phrase "vice versa" has been cancelled and the meaning of that phrase spelled out to clearly point out and distinctly claim the subject matter. It is believed that the objection to claims 7, 26, and 32 has now been overcome.

In the Office action, claims 1-8, 20, 26, 32-34, and 37-38 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,134,311 to Biber et al. ("Biber"). It is respectfully submitted that the examiner has misconstrued the teachings of Biber.

It is the examiner's position, regarding claim 1, that "Biber discloses a method of correcting impedance curvature in a MOS driver circuit (circuit in Fig. 3)." That statement is incorrect. Biber is not directed to a method of correcting impedance curvature. Rather, Biber is directed to a method of impedance matching. See abstract, first line. See also, claim 1 of Biber which recites "a self-adjusting impedance matching driver."

Further, the examiner cites Biber as disclosing "operating said first MOS transistor and said second MOS transistor so as to compensate for changes in output impedance of said first MOS transistor through corresponding changes in output impedance of said second MOS transistor." The examiner cites the abstract of Biber, as well as column 4, the paragraph beginning at line 49. Biber, however, does not teach or suggest compensating for changes in the impedance of one transistor by implementing corresponding changes in another transistor. Rather, Biber speaks of adding transistors to the primary driver devices 42, 44 so as to change the overall impedance of the circuit.

> The primary driver devices 42, 44 have a characteristic impedance equal to the highest anticipated impedance to be presented under normal conditions by load 40. Each of the pairs of devices just described has a preselected characteristic impedance which, *when added in parallel to the impedance of devices 42 and 44, as the case may be, serves to reduce the characteristic impedance of the output stage 32 in a selectable manner.* The addition or omission of the pairs of devices just described, referred to herein as

> "incremental impedance pairs," or "incremental impedance devices," is controlled by the operation of the set of latches 36 under control of the control logic 38, in a manner which is described below.(emphasis added) (column 3, lines 51 – 64)

The paragraph cited by the examiner refers to Fig 3, and speaks of incremental impedances being provided. As seen more clearly in Fig. 4, Fig. 4 illustrates the different resistances which can be added to the resistance of the main drivers. Thus, it is clear from an examination of Fig. 3 in combination with Fig. 4, that the individual impedance of transistors is not being manipulated. Rather, transistors are being added to or subtracted from the output stage so that the overall impedance of the driver can be matched to the load. It is respectfully submitted that Biber neither anticipates nor renders obvious the subject matter of claim 1.

Claim 7 recites operating the first and second transistors "so as to increase output impedance of said second MOS transistor when output impedance of said first MOS transistor decreases, and to decrease output impedance of said second MOS transistor when output impedance of said first MOS transistor increases." Again, Biber is silent about modifying the impedance of individual transistors such that it is believed that claim 7 is in condition for allowance.

Independent claims 20 and 37 recite subject matter similar to independent claim 1. Thus, for the same reasons that claim 1 is in condition for allowance, independent claims 20 and 37 are in condition for allowance.

Independent claims 26 and 32 recite subject matter similar to independent claim 7. Accordingly, for the same reasons that independent claim 7 is in condition for allowance, claims 26 and 32 are also believed to be in condition for allowance.

Certain additional changes have been made to the claims as a matter of style – more particulary, to insure that each each dependentt method claim further defines the method.

In a restriction requirement mailed 2 September 2005 in the instant application, it was noted that upon the allowance of a generic claim, applicant would be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the

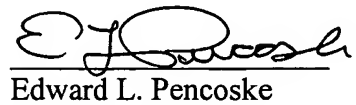
limitations of an allowed generic claim as provided by 37 C.F.R. 1.141. Accordingly, applicant resubmits previously withdrawn dependant claims 9-19, 21-25, 27- 31, 35, and 36. These dependent claims are believed to satisfy the requirements of 37 C.F.R. 1.141. Furthermore, all of these dependant claims depend directly or indirectly from an independent claim which is believed to be in condition for allowance.

Also resubmitted are independent claims 64 and 65. Independent claim 64 is a system claim which is similar to allowable claim 37 whereas independent claim 65 is a system claim similar to independent claim 32. System claims 64 and 65 are also believed to meet the requirements of 37 C.F.R. 1.141.

Withdrawn claims 46-63 have been cancelled without prejudice. It is applicant's intention to resubmit claims 46-63 in a divisional application.

Applicant has made a diligent effort to place the instant application in condition for allowance. Accordingly, a Notice of Allowance for claims 1, 2, 4, 5, 7-9, 11, 13-15, 17-45, 64, and 65 is respectfully requested. If the examiner is of the opinion that the aforementioned claims are not in condition for allowance, the examiner is respectfully requested to contact applicant's attorney at the number listed below.

Respectfully submitted,



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Date: 22 June 2006